CLAIMS

What is claimed is:

1. A transport processor comprising:

a front end to receive multiple transport streams, each transport stream including a plurality of packets, the front end comprising a packet processor to create an aggregate transport stream;

a memory to store the aggregate transport stream.

2. The transport processor of claim 1, wherein the number of streams within the aggregate transport stream is scaleable.

3. The transport processor of claim 1, wherein the front end further comprises:

a PID filter to discard packets in the aggregate transport stream prior to processing, in order to minimize memory bandwidth and improve descrambling and demultiplexing throughput.

4. The transport processor of claim 1, wherein the aggregation of transport streams permits the use of a single PID filter, a single descrambler, and a single demultiplexer.

5. The transport processor of claim 1, further comprising:

a descrambler to descramble the packets in the aggregate transport stream.

6. The descrambler in the transport processor of claim 5, further comprising:

a packet level control and key RAM control logic to select a descrambling standard for a packet within the aggregate transport stream; and

a decryption circuit to descramble the packet using the selected descrambling standard.

7. The transport processor of claim 1, further comprising:

the packet processor to format each packet from multiple streams to a common format, the common format including originating stream information.

8. The transport processor of claim 7, wherein the common format is a 208-byte format, and smaller packets are padded to create this common format.

9. The transport processor of claim 7, wherein the originating stream information comprises temporal information.

10. The transport processor of claim 7, wherein the originating stream information comprises stream identifier and additional user specified information.

11. The transport processor of claim 1, wherein the aggregate stream includes transport data obtained from different transport protocol standards.

12. The transport processor of claim 1, further comprising:

a plurality of input/output (I/O) ports;

an I/O port that is user-selectable to a parallel or serial format.

13. The I/O ports in the transport processor of claim 12, further comprising:

a serial output block to resample parallel data, and to convert the parallel data to serial data with an independently programmable bit clock selection.

14. The transport processor of claim 1, further comprising:

a PID filter to discard packets from the aggregate transport stream, retaining only packets of interest;

a descrambler to descramble the remaining packets in the aggregate stream; and

a demultiplexer to demultiplex the descrambled packets in the aggregate stream;

wherein the descrambler and the demultiplexer receive only the packets of interest.

15. The transport processor of claim 1, further comprising:

a switching matrix to select a subset of the streams out of a plurality of streams for storage and subsequent descrambling and demultiplexing.

16. The switching matrix in the transport processor of claim 15, further comprising:

a delay circuit to switch to a new stream after receiving an end of packet signal from an original stream, such that only complete packets from the original stream are propagated.

17. The switching matrix in the transport processor of claim 16, further comprising:

a data valid signal to indicate that the output of the switching matrix is valid only after an end of packet signal is received from the new stream, such that only complete packets from the new stream are propagated.

18. A system on a chip (SOC) comprising:

a transport processor to PID filter, descramble, and demultiplex a plurality of transport streams;

a memory to store demultiplexed outputs of the plurality of transport streams; and

an output processor to retrieve one or more demultiplexed outputs from the memory and perform audio/video decode and display functions simultaneously.

19. The SOC of claim 18, wherein the output processor is a combination of digital audio decoder, digital video decoder, audio processor, and display processor.

20. The SOC of claim 19, wherein the audio and video frames for two independent transport streams are rendered without repeated or skipped frames.

21. The SOC of claim 18, wherein the transport processor comprises:

a front end to receive multiple transport streams, each transport stream including a plurality of packets, the front end comprising a packet processor to create an aggregate transport stream; and

a readback logic to read packets from the memory, for descrambling and demultiplexing functions.

22. The SOC of claim 18, further comprising a memory interface to access the contents of the memory, the memory interface used by the transport processor and the output processor.

23. In a transport processor a front end to receive a plurality of transport streams from multiple digital receivers, the front end comprising:

a switching matrix to receive the plurality of transport streams and to output a programmable subset of the plurality of transport streams;

a packet processor to receive the subset of the plurality of transport streams and to aggregate the subset of the plurality of streams into a single aggregate transport stream.

24. The front end of claim 23, further comprising:

a memory to store the aggregate transport stream.

25. The front end of claim 24, further comprising:

a PID filter to discard packets, retaining only packets of interest.

26. The front end of claim 24, further comprising:

an external input/output (I/O) to receive the plurality of transport streams, the external I/O having a plurality of bi-directional ports.

27. The front end of claim 26, wherein each of the bi-directional ports can be configured as either a single parallel or a pair of serial ports.

28. The front end of claim 27, wherein a bi-directional port includes a serial input block to receive serial input and generate a synchronized parallel output.

29. The front end of claim 27, wherein a bi-directional port includes a serial output block to generate a serial transport stream with an independent bit clock for output.

30. The front end of claim 23, wherein the switching matrix comprises:

a stream select delay unit to ensure that only compete packets are propagated.

31. The front end of claim 23, wherein the packet processor is further to attach appropriate header and footer information to transport packets in the subset of the plurality of transport streams.

32, The pocket processor in the front end of claim 31, wherein the packet processor generates packets of a uniform size, regardless of originating protocol.